Amendments to the Specification

Please amend paragraphs [0009] and [0010] as follows:

[0009] According to one aspect of the present invention, a memory system ~~system~~ includes a SIMM which contains at least one memory device and a signal transmission line connected between the at least one memory device and a connection terminal, and a DIMM which contains at least two memory devices and a signal transmission line connected between the at least two memory devices and a connection terminal, where a length of the signal ~~tranmission~~ transmission line of the SIMM is longer than a length of the signal transmission line of the DIMM. The load of the memory devices of the SIMM is less than the load of memory devices of the DIMM, and the longer length of the signal ~~tranmission~~ transmission line of the SIMM increases a signal delay time of the SIMM to compensate for the different loads of the SIMM and DIMM memory devices. The memory system may further include a first socket which receives the connection terminal of the SIMM, a second socket which receives the connection terminal of the DIMM, and a signal transmission line connected between the first and second sockets, and the longer length of the signal ~~tranmission~~ transmission line of the SIMM may further compensate for the signal transmission line connected between the first and second sockets.

[0010] According to another aspect of the present invention, a memory system includes a memory controller, a first memory module including at least one first memory device having a first load and a first signal transmission line connected between the at least one first memory device and a connection terminal, a second memory module including at least one second memory device having a second load and a second signal transmission line connected between the at least

one second memory device and a connection terminal, and first and second sockets which are connected to the memory controller and which respectively receive the connection terminals of the first and second memory modules. The first load of the at least one first memory device is less than the second load of the at least one second memory device, and a length of the first signal ~~tranmission~~ transmission line of the first memory module is longer than a length of the second signal transmission line of the second memory module. The longer length of the first signal ~~tranmission~~ transmission line of the first memory module increases a signal delay time of the first memory module to compensate for the different loads of the first and second memory modules. Also, the longer length of the first signal ~~tranmission~~ transmission line of the first memory module may further compensate for the ~~precense~~ presence of another transmission line connected between the first and second sockets.